Electronic Version
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Claims

[c1] 1. A chip package structure, comprising:
a carrier;
a chip, having an active surface with a plurality of bumps thereon, wherein the active surface of the chip is bonded to the carrier using a flip-chip bonding technique so that the chip and the carrier are electrically connected; and
an encapsulating material layer, covering the chip and the carrier and filling the bonding gap between the chip and the carrier, wherein the encapsulating material layer between the chip and the carrier has a first thickness and the encapsulating material layer on the chip has a second thickness such that the second thickness is between 0.5 ~ 2 times the first thickness.

[c2] 2. The chip package structure of claim 1, wherein maximum diameter of particles constituting the encapsulating material layer is smaller than 0.5 times the first thickness.

[c3] 3. The chip package structure of claim 1, wherein the package further comprises an array of solder balls attached to a surface of the carrier away from the chip.

[c4] 4. The chip package structure of claim 1, wherein the package further comprises a passive component attached and electrically to the carrier.

[c5] 5. The chip package structure of claim 1, wherein the carrier is selected from a group consisting of a package substrate and a lead frame.

[c6] 6. A chip package structure, comprising:
a carrier;
a chipset, set on and electrically connected to the carrier, wherein the chipset comprises a plurality of chips, at least one of the chips is bonded to the carrier or another chip using a flip-chip bonding technique so that a flip-chip bonding gap is created; and
an encapsulating material layer, completely filling the flip-chip bonding gap and covering the chipset and the carrier, wherein the encapsulating material layer within the flip-chip bonding gap has a first thickness and the encapsulating material layer on the chipset has a second thickness such that the second thickness is between 0.5 ~ 2 times the first thickness.

[c7] 7. The chip package structure of claim 6, wherein maximum diameter of particles constituting the encapsulating material layer is smaller than 0.5 times the first thickness.

[c8] 8. The chip package structure of claim 6, wherein the chipset at least comprises:
a first chip, having a first active surface, wherein the first chip is attached to the carrier such that the first active surface is positioned away from the carrier; and
a second chip, having a second active surface with a plurality of bumps thereon, wherein the second active surface of the second chip is bonded and electrically connected to the first chip using a flip-chip bonding technique such that the bumps between the second chip and the first chip set a flip-chip bonding gap.

[c9] 9. The chip package structure of claim 8, wherein the chipset further comprises a plurality of conductive wires with ends electrically connected to the first chip and the carrier respectively.

[c10] 10. The chip package structure of claim 6, wherein the chipset at least comprises:
a first chip, having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier using a flip-chip bonding technique such that the first bumps between the first chip and the carrier set a flip-chip bonding gap;
a second chip, having a second active surface, wherein

the second chip is attached to the first chip such that the second active surface is positioned away from the first chip; and

a third chip, having a third active surface with a plurality of second bumps thereon, wherein the third active surface of the third chip is bonded and electrically connected to the second chip using a flip-chip bonding technique such that the second bumps between the third chip and the second chip set another flip-chip bonding gap.

[c11] 11. The chip package structure of claim 10, wherein the chipset further comprises a plurality of conductive wires with ends electrically connected to the second chip and the carrier respectively.

[c12] 12. The chip package structure of claim 6, wherein the package further comprises a passive component attached and electrically connected to the carrier.

[c13] 13. The chip package structure of claim 6, wherein the package further comprises an array of solder balls attached to a surface of the carrier away from the chips.

[c14] 14. The chip package structure of claim 6, wherein the carrier is selected from a group consisting of a package substrate or a lead frame.

[c15] 15. A chip packaging process, comprising the steps of:
providing a carrier a plurality of chips such that each chip has an active surface and at least one of the active surfaces has a plurality of bumps thereon;
connecting the chips and the carrier together electrically; and
forming an encapsulating material layer over the chips and the carrier and filling the gap between the chips and the carrier, wherein the encapsulating material layer between the chips and the carrier has a first thickness and the encapsulating material layer over the chips has a second thickness such that the second thickness is between 0.5 to 2 times the first thickness.

[c16] 16. The process of claim 15, wherein the step of forming the encapsulating material layer comprises performing a reduced-pressure transfer molding process.

[c17] 17. The process of claim 16, wherein after forming the encapsulating material layer, further comprises cutting the carrier to form a plurality of chip package structures.

[c18] 18. The process of claim 16, wherein the reduced-pressure transfer molding process is carried out at a pressure below 20 mm-Hg.

[c19] 19. The process of claim 16, wherein the reduced-pres-

sure transfer molding process is carried out at a temperature at least 10°C below the melting point of the bumps.

[c20] 20. The process of claim 16, wherein maximum diameter of particles constituting the encapsulating material layer is smaller than 0.5 times the first thickness.